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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,064	07/07/2003	Young-chan Kweon	SEC.316REC	1389
20987	7590	12/08/2004	EXAMINER	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			SCHILLINGER, LAURA M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/613,064	Applicant(s) KWEON, YOUNG-CHAN	
	Examiner Laura M Schillinger	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) 1-15, 23-28, 30-38 and 42-49 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-22, 29 and 38-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/770,796.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/31/03; 7/7/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

Claims 1-15, 23-28, 30-37, 42-49 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/23/04.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16-22, 29, 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Kato et al -US 5054887) in further view of Miyago et al ('370).

Applicant's admitted prior art (Kato et al -US 5054887) teaches all the following claimed limitations, the citations refer to Applicant's specification as follows :

16. A TFT substrate, comprising:

a gate electrode comprising a first metal film over a substrate (Col.1, lines: 40-50);

a gate pad (gate bus lines) consisting the first metal film (Col.1, lines: 50-56);

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an insulated film over the gate electrode and having an exposed area of the first metal film over the gate pad (Col.1, lines: 56-65);

a semiconductor film pattern over the insulated film (Col.1, lines: 60-65)

a source electrode formed over a first portion of the semiconductor film pattern (Col.2, lines: 5-10);

a drain electrode formed over a second portion of the semiconductor film pattern (Col.2, lines: 5-10;

a passivation film pattern formed over the source electrode, having a contact hole over the drain electrode and having an exposed area of the first metal film of the gate pad (Col.2, lines: 15-25);

a first pixel electrode pattern electrically contacted to the drain electrode on the passivation film pattern (Col.2, lines: 25-30); and

a second pixel electrode pattern electrically contacted to the exposed area of the first metal film of the gate pad (Col.2, lines: 25-30).

21. Applicant's admitted prior art ('887) teaches A TFT substrate. as recited in claim 16, wherein the first and second pixel patterns comprise ITO (Col.2, lines: 25-30).

22. Applicant's admitted prior art ('887) teaches A TFT substrate, as recited in claim 16, wherein a portion of the passivation film directly contacts the semiconductor film pattern (Col.2, lines: 15-20).

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29. Applicant's admitted prior art ('887) teaches a TFT substrate, as recited in claim 16, wherein a portion of the passivation film directly contacts the semiconductor film pattern (Col.2, lines: 15-20).

40. Applicant's admitted prior art ('887) teaches a TFT substrate as in claim 16, wherein the semiconductor film pattern comprises: an amorphous silicon film on the insulated film; and a doped amorphous silicon film on the amorphous silicon film (Col.1, lines: 55-65).

41. Applicant's admitted prior art ('887) teaches A TFT substrate as in claim 16, wherein the second pixel electrode pattern contacts portions of the exposed gate pad (Col.2, lines: 30-35).

However, Applicant's admitted prior art ('887) fails to teach additional limitations of claim 16 as follows:

A gate electrode comprising a first metal film over a substrate and a **second metal film over the first metal film;**

A gate pad consisting of the first metal film and a **portion of a removed area of the second metal film.**

Miyago et al ('370) teaches a similar method to Applicant's admitted prior art ('887) and further teaches to form a second metal layer as part of the gate electrode (Col.3-4, lines: 60-10).

Moreover, Miyago teaches that the gate pad area consist of a first metal film and a portion of a removed area of the second metal film (Fig.1 (12 and 3)).

17. Miyago teaches a TFT substrate, as recited in claim 16, wherein the first metal film comprises a refractory metal (Col.3, lines: 60-65).

18. Miyago teaches A TFT substrate. as recited in claim 17. wherein the first metal film comprises a material selected from the group consisting of Cr, Ta, Mo, and Ti (Mo- Col.3, lines: 60-65).

19. Miyago teaches A TFT substrate. as recited in claim 16, wherein the second metal film comprises Al or an Al alloy (Col.3, lines:60-65).

20. Miyago and Applicant's admitted prior art ('887) teaches A TFT substrate. as recited in claim 16, wherein the insulated film comprises a nitride film SiN (See respectively, Col.4, lines: 25-30 and Col.1, lines: 55-60) .

38. Miyago teaches A TFT substrate as in claim 16, wherein at least one of the first and the second metal film of the gate electrode and the gate pad has tapered-sidewalls (Fig.2 (4a and 4b).

39. Miyago teaches a TFT substrate as in claim 38, wherein the second metal film has tapered sidewalls(Fig.2 (4a and 4b).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art (Kato '887) to further include the two metal layer gate structure taught by Miyago because as Miyago teaches the dual structure protects from hillocks and furthermore ensures that source and gate wirings are kept safe from breakage (Col.5, lines: 1-17).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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*Laura M. Schley*  
LMS

12/5/04